Location, Conditions and Important Deadlines

Conference Location

Europole Centre de congrès
World Trade Center Grenoble
5-7 place Robert Schuman, 38000 Grenoble
http://www.europole-congres.com

For the location map and travel information please visit the web page.

Conference Fee

The fee includes all technical sessions, all meals , abstract volume and conference proceedings.
A special event reception held at the Modern Museum of Grenoble is also covered.

Advanced registration (deadline February 1, 2006):	**550 €**
Late registration (after February 1, 2006):	**600 €**
On-site registration:	**650 €**

Refund policy:
Any cancellation made before February 1, 2006 is subject to a refund processing fee of 30 €. Refunds requested after February 1 are subject to a 100 € cancellation fee. No refunds will be made after February 25, 2006. Substitutions between participants may be made at any time.

Registration / Payment

Payment can be made by bank transfer, cheque or credit cards (VISA & MASTERCARD). For details please refer to the MAM 2006 web site. Conference registration will become effective only after receiving the payment.
Please register on the MAM 2006 page.

Exhibition

During the conference a vendor display / exhibition will be organised for companies and institutions to present their products and services. For more information please send a request.

Deadlines

Abstracts are due: November 14, 2005
Notification of authors: December 2005
Submission of papers: March 6-7, 2006

Committee members and Contact address

Scientific Program Committee

T. Gessner	TU Chemnitz, Germany
D. Gravesteijn	Philips Research Leuven, Belgium
H. Körner	Infineon Technologies AG, Germany
R. Madar	INP Grenoble-CNRS, France
S. Mantl	Forschungszentrum Jülich, Germany
T. Marangon	STMicroelectronics, Italy
S. Peterson	Royal Institute of Technology, Sweden
Y. Shacham- Diamand	University of Tel Aviv, Israel
I. Suni	VTT, Espoo, Finland
J. Torres	STMicroelectronics, France
M. Van Hove	IMEC, Leuven, Belgium
E. Zschech	AMD Saxony, Dresden, Germany

Local Organizing Committee

V. Arnal	STMicroelectronics, France
L. Arnaud	CEA-LETI, France
E. Blanquet	INP Grenoble-LTPCM, France
B. Chenevier	INP Grenoble-LMGP, France
T. Chevolleau	CNRS-LTM, France
C. Goldberg	Freescale Crolles, France
L. Gosset	Philips Crolles, France
O. Joubert	CNRS-LTM, France
C. Lartigue	INP Grenoble, France
D. Louis	CEA-LETI, France
T. Marangon	STMicroelectronics, Italy
R. Madar	INP Grenoble-CNRS, France
S. Maitrejean	CEA-LETI, France
O. Thomas	Univ. P. Cezanne, France
J. Torres	STMicroelectronics, France

Conference Schedule

Sunday, March 5	
Conference registration	18:00 - 20:00
Reception	20:00 - 22:00
Monday, March 6	
Conference registration	8:00 - 9:00
Technical session	9:00 - 16:00
Special event reception at the Museum	19:00 - 22:00
Tuesday, March 7	
Conference registration	8:00 - 9:00
Technical session	9:00 - 17:00
Conference Dinner	19:00 - 21:00
Wednesday, March 8	
Technical session	9:00 - 12:00

Optional visit in the afternoon to MINATEC, French Centre for Innovation in micro & nanotechnologies.

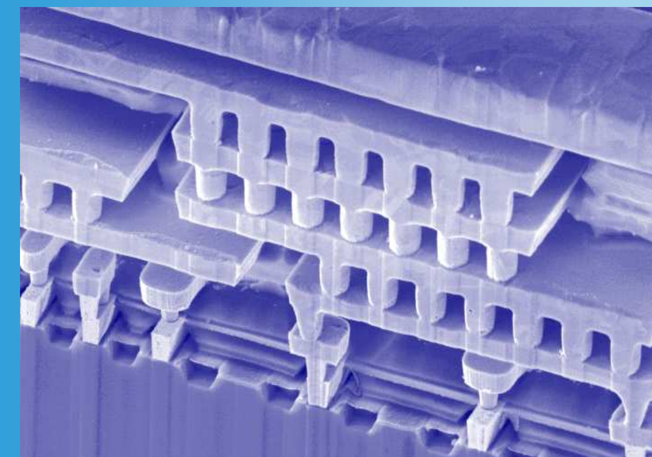
Contact
Email: mam-conference@inpg.fr
+33 (0)4 76 51 34 29

MATERIALS FOR ADVANCED METALLIZATION

MAM2006

A single-session workshop featuring
Materials and Structures
for Advanced Micro- and Nanoelectronics

FINAL ANNOUNCEMENT



Materials and structures for advanced micro- and nanoelectronics
Basics and fundamental studies
Metallization (IC and other applications)
Low k and ULK dielectrics
Silicides
Nanoscale interconnects
Integrated passives
Modeling and simulation
Reliability, lifetime and analyticaltechniques
Interconnect related packaging issues

www.mam-conference.org

Scope of the Conference and Invited Speakers

This workshop is the 15th in a series devoted to materials research, materials properties and interactions. Starting as workshop on refractory metals and silicides in the 80ies, moving to materials for advanced metallization in 1995, this year workshop will include new and challenging topics in the field of BEOL-45nm solutions and 32nm explorative work.

The objective of the workshop is to provide a forum for open discussions between science and industrial application. It is dedi- cated to materials scientists, process and integration engineers.

Topics include both fundamental and applied research, as well as issues related to introduction into manufacturing. With the progressive scaling down of device dimensions and the simultaneous demands for more functionality, the challenges have become tremendous. New and extensive materials research is needed to further follow IC scaling as well as to develop new devices on the nanoscale. Therefore this workshop is organised in cooperation with several European R&D projects active in the field (NANOCMOS, SINANO…) and will address the preliminary results that have been achieved.

Invited speakers

Invited talks will be given by scientific and technical leaders in each of the key areas to present the current state-of-the-art and to stimulate technical discussions.

B. MILNE - **Cambridge (UK)** - Near and long term electronic applications of CNT

S. LIST – **INTEL** - Benchmarking Advanced Interconnect Options and Challenges

DAUSKARDT – **Stanford** - Nanostructured low- k materials and the effects of process environments on reliability

C. LAVOIE - **IBM** - Nickel silicide phase stability

C. HSIA - **TSMC -** Materilas & process developments for 45nm at TSMC

P. ANCEY - **STMicroelectronics** - Above IC: materials and processes

I. ZIENERT – **AMD** – Overburden effect on grain size and texture – a way to improve copper reliability?

H. HUEBNER *et al* – **Infineon** – Micro contacts with sub-30µm pitch for 3D chip on chip integration

P. STOLK / M. WOO – **Philips/ Freescale** – Integration for advanced technology nodes

O. THOMAS – **Univ. P. Cézanne –TECSEN** - Stress development during silicidation: from average to local stress

O. JOUBERT – **CNRS** – Etching (low- k and metal) and stripping

J. GAMBINO – **IBM** microelectronics – Optimization of Self Aligned barrier integration: from the 4 nm node to the CMOS Image sensor Technology

M. BRILLOUET – **LETI** - Keynote

Topics of Materials for Advanced Metallization

MAM2006

Materials and Structures for Advanced Micro- and Nanoelectronics

- Strained Silicon / SiGe
- Nanowires / Carbon nanotubes (CNT)
- Metallic nano-dots
- Metallization aspects of molecular electronics: metal-molecule interfacing, electron injection into molecular wires

Basics and fundamental studies

- Kinetics and thermodynamics of reactions
- Precursor chemistry and delivery

Metallization

- Metal gates, electrodes for high k dielectrics and capacitors
- Copper interconnects: deposition, properties, integration
- Advanced Al and non-Cu metallization
- Diffusion barriers: advanced materials and deposition methods, material interaction, barrier performance
- Electrochemical/electroless processes: seedless deposition, seed layer repair approaches, grain size and morphology engineering
- New metallization materials for MRAM, FeRAM…
- Interconnects for surface acoustic wave (SAW) devices
- High temperature metallization (sensors…)
- MEMS / NEMS related metallization issues

Low k and ULK dielectrics (dense and porous)

- Deposition process & equipment
- Properties & characterization
- Patterning: etch, strip, hardmasks
- Integration challenges: interactions with materials and processes, adhesion…
- Air gap structures
- Porosity related issues: pore sealing, cap layers, mechanical strength

Silicides

- Advanced silicides and salicides for gate & source / drain
- Growth, properties, integration
- Silicides for alternative applications

Nanoscale Interconnects

- Size effects, morphology studies
- Research on understanding and improving resistance increase of narrow Cu lines

Shrinking of conventional interconnects

Multilevel Metallization

- Damascene / Dual Damascene
- RIE and other subtractive approaches
- CMP of metals and dielectrics: New CMP materials and processes, CMP related cleaning and defectivity issues, Electrochemical polishing, Advanced endpoint detection
- Integration issues of Cu/low k and Al/low k in MLM systems
- Optical interconnects
- RF / wireless interconnects
- X-architecture design

Integrated Passives

- Capacitors: electrodes, insulator
- Inductors / coils
- Precision metal resistors, new materials and integration
- Integration and assessment
- On-chip integrated, in package integrated…

Modeling / Simulation

- Of processes, equipment, interconnect systems, material properties

Reliability, Lifetime and Analytical Techniques Related to Interconnects and Dielectrics

- Electromigration
- Stressmigration
- Void formation mechanisms and detection
- Acoustomigration in SAW device metallization
- Dielectrics: breakdown, leakage, BTS, charges, drift of k-value
- New failure types and failure distribution evaluation
- Extrapolation models and lifetime prediction for new materials and integration schemes
- Interconnect / packaging interaction related reliability
- Advanced analytical techniques for material and Interconnect characterization

Interconnect related packaging issues

- FlipChip, 3D interconnects, wafer on wafer and chip on chip approaches
- Redistribution layers and materials
- System on chip, system in package
- Low-k related packaging issues

Abstracts and Papers

Abstracts should be submitted in a 2-page format, with the first page text and the second page accompanying tables and figures. Minimum font size should be at least 10. Affiliation, address and email of the corresponding author should be included.

Abstracts should be submitted as pdf or word file by email at : **mam-conference@inpg.fr**

Full-length papers will be published in a special issue of *Microelectronic Engineering*